Errata Version 1.0
SL811HS/SL811S
Silicon Revision 1.5

1. Host Mode: SE0 Problem in Low Speed Hub Operation

Description: Some hubs that send SE0s upstream during the EOF1 time frame may cause the SL811HS to stop sending SOFs. This problem occurs in some instances when operating with low speed devices attached downstream of such a Hub. This is not a problem with full speed devices.

According to USB spec, hubs are permitted to transmit SE0s during the EOF1 time frame. This is done to eliminate potential babble conditions on the bus and is an optional feature implemented in some hubs.

Implication: The SL811HS can not host a low speed device downstream of a hub that generates SE0s during EOF1.

Workaround: The only complete workaround is to use a hub that does not transmit SE0s upstream during EOF1.

Some hubs, such as all of Cypress' hubs, have the option to disable SE0s from being generated during EOF1.

For a list of hubs that do not generate SE0s upstream during EOF1, or for more information on disabling this feature in Cypress hubs, please contact Cypress USB support.

Note: Hub support is not required for OTG dual role devices (DRDs).

Status: Closed

2. Host Mode: Sync to SOF Does Not Apply to Low Speed Mode

Description: The SYNC to SOF bit (bit 5) of the USB Host Control Registers [00H, 08H], is only designed for full speed support. However, all other full speed SOF bits and registers do apply to low speed EOPs as well.

In full speed mode, this bit should only be used when the software can not fit a packet within the remaining 1ms frame. Setting this bit will automatically delay sending the packet until the next SOF.

Implication: If the SOF bit is set when operating in low speed mode, packets may not get sent from the SL811HS.

Workaround: Do not set the SOF bit when operating in low speed mode. Instead, if a packet doesn't fit within the remaining 1ms frame, firmware needs to delay sending it until after the next EOP. Using a simple delay loop or pulling the SOF Timer interrupt (also EOP Timer interrupt in low speed mode) are two possible ways of doing this.

Status: Closed

3. Host/Peripheral Mode: 12MHz Operation with Sensitive Internal PLL

Description: The internal PLL is very sensitive. The PLL will cause any high frequency noise on the VDD pins to result in clock jitter.

Implication: When operating the SL811HS at 12MHz, high frequency noise on the VDD pins could result in clock jitter. The clock jitter could cause result in a number of different symptoms depending on the severity of the jitter. Most notably will be improper USB data signaling at full speed and improper timing of SOF packets.

Workaround: The best workaround is to use 48MHz to eliminate using the PLL. If 12MHz is required there are a number of things that can be done to reduce any jitter output of the PLL.

1. Reduce high frequency noise on all SL811HS VDD pins. This can be accomplished by adding proper decoupling capacitors directly on the VDD pins. The value of 0.1uF might be too large, depending on the inductivity of the traces on the PCB and values of 0.01uF or even 1000pF should be experimented with. In addition ceramic capacitors are recommended.

2. Use a 12MHz oscillator rather then a crystal. An oscillator produces much sharper edge rates, which will allow more tolerance for jitter.

3. Careful layout can minimize this PLL jitter significantly:
   a. Use the shortest traces possible for decoupling capacitors.
   b. Use ground and VCC planes.

Status: Closed

4. Peripheral Mode: DMA Interface

Description: The DMA interface is unreliable.

Implication: When performing DMA writes, data may get corrupted. This problem has only been seen for DMA write operations, but may occur for read operations as well.

Workaround: Use the standard Data Port interface instead of the DMA interface.

Status: Under Investigation

Revision History

Revision	Date Issue	Change
1.0	April 1, 2003	1. Created for silicon revision 1.5 only 2. Added DMA Interface item