FAIRCHILD SEMICONDUCTOR™

August 1993
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74VHC164
8-Bit Serial-In, Parallel-Out Shift Register

General Description

The VHC164 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC164 is a high-speed 8-Bit Serial-In/Parallel-Out Shift Register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

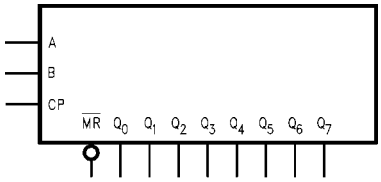
- High Speed: f_{MAX} = 175 MHz at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection provided on all inputs
- Low noise: V_{OLP} = 0.8V (max)
- Pin and function compatible with 74HC164

Ordering Code:

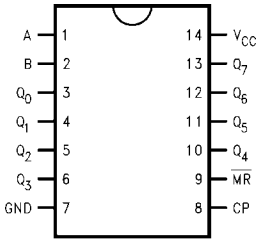
Order Number	Package Number	Package Description
74VHC164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC164SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC164MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0–Q_7	Outputs

Functional Description

The VHC164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other input. An unused input must be tied HIGH.

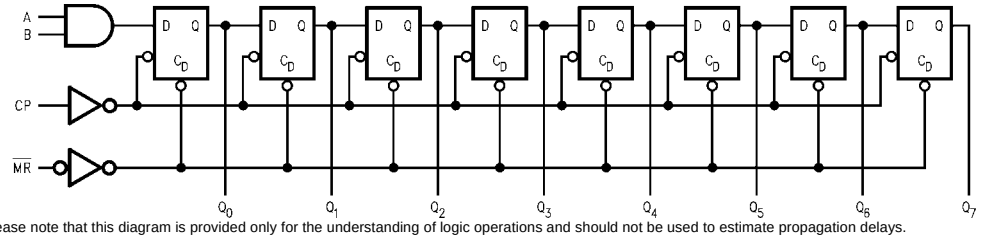
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Function Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L–L
Shift	H	L	L	L	Q_0–Q_6
	H	L	H	L	Q_0–Q_6
	H	H	L	L	Q_0–Q_6
	H	H	H	H	Q_0–Q_6

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Immaterial
Q = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to + 7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
DC Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ns/V ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V ~ 20 ns/V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0– 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8	V	C_L = 50 pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	0.8	V	C_L = 50 pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	80	125		65		MHz	C_L = 15 pF, R_L = 1k
			50	75		45			C_L = 50 pF, R_L = 1k
		5.0 ± 0.5	125	175		105		MHz	C_L = 15 pF, R_L = 1k
			85	115		75			C_L = 50 pF, R_L = 1k
t_{PLH}	Propagation Delay	3.3 ± 0.3		8.4	12.8	1.0	15.0	ns	C_L = 15 pF, R_L = 1k
t_{PHL}	Time (CP–Q_n)			10.9	16.3	1.0	18.5		C_L = 50 pF, R_L = 1k
		5.0 ± 0.5		5.8	9.0	1.0	10.5	ns	C_L = 15 pF, R_L = 1k
				7.3	11.0	1.0	12.5		C_L = 50 pF, R_L = 1k
t_{PHL}	Propagation Delay	3.3 ± 0.3		8.3	12.8	1.0	15.0	ns	C_L = 15 pF, R_L = 1k
	Time ($\overline{MR}$–Q_n)			10.8	16.3	1.0	18.5		C_L = 50 pF, R_L = 1k
		5.0 ± 0.5		5.2	8.6	1.0	10.0	ns	C_L = 15 pF, R_L = 1k
				6.7	10.6	1.0	12.0		C_L = 50 pF, R_L = 1k
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			76				pF	(Note 4)

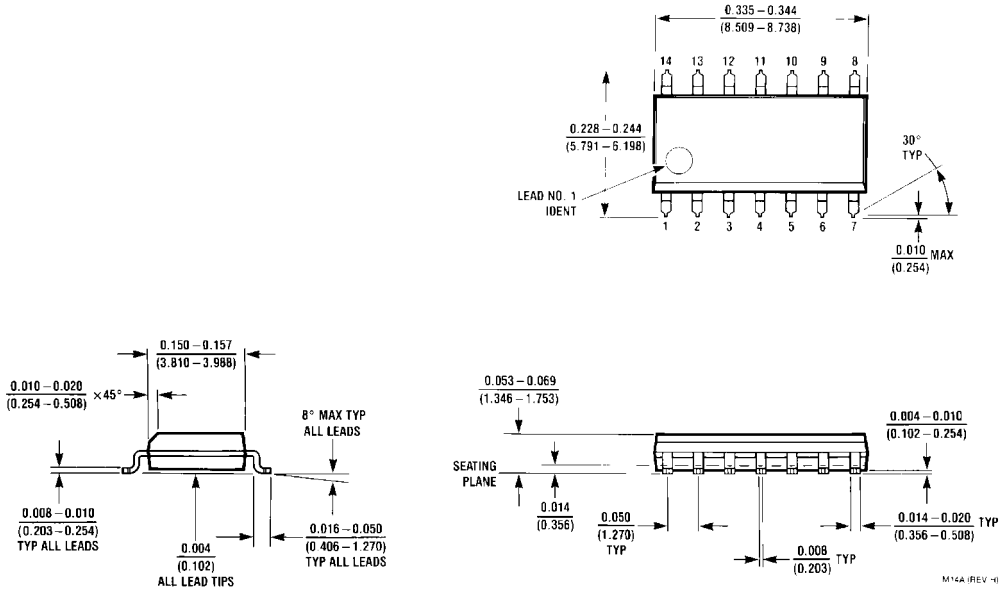
Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 5)	T_A = 25°C	T_A = −40°C to +85°C		Units
			Typ	Guaranteed Minimum		
t_W(L)	Minimum Pulse Width (CP)	3.3		5.0	5.0	ns
t_W(H)		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		5.0	6.0	ns
		5.0		4.5	4.5	
t_H	Minimum Hold Time	3.3		0.0	0.0	ns
		5.0		1.0	1.0	
t_{REC}	Minimum Removal Time ($\overline{MR}$)	3.3		2.5	2.5	ns
		5.0		2.5	2.5	

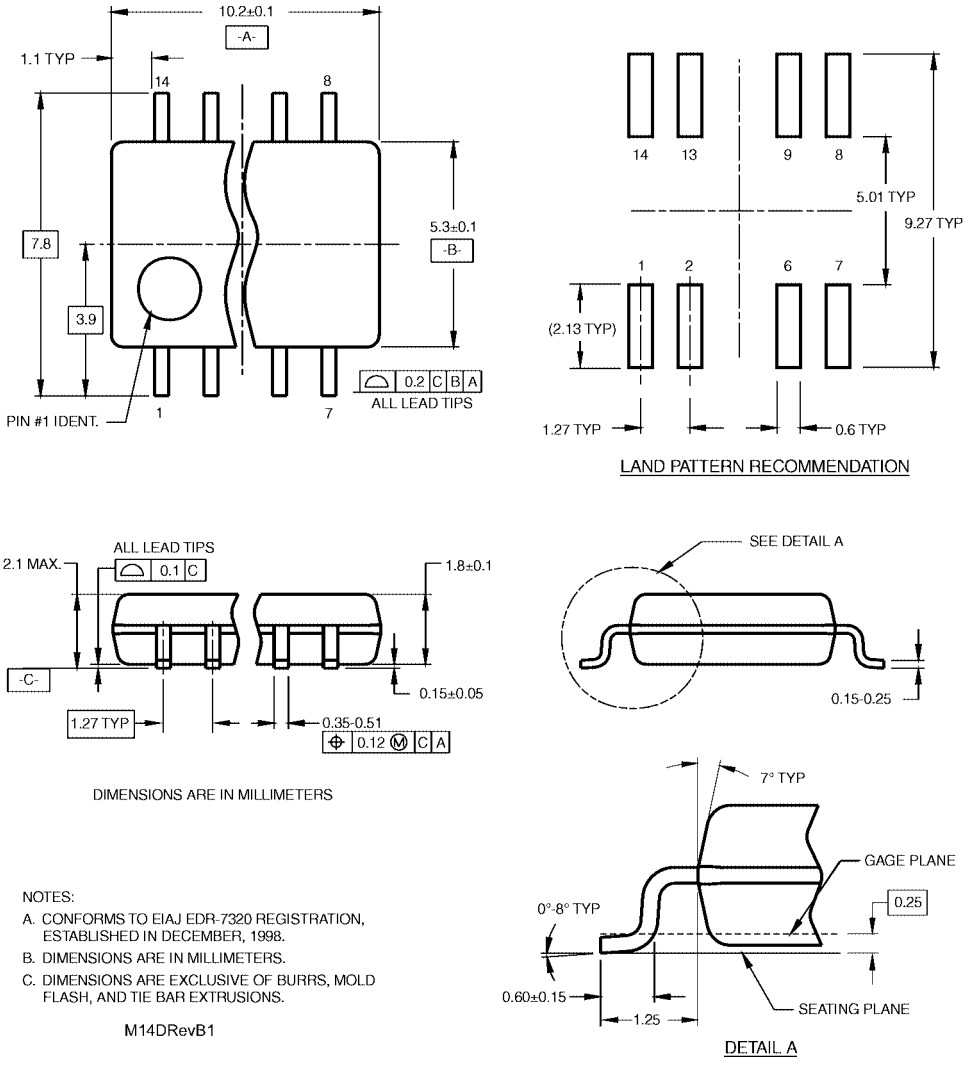
Note 5: V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

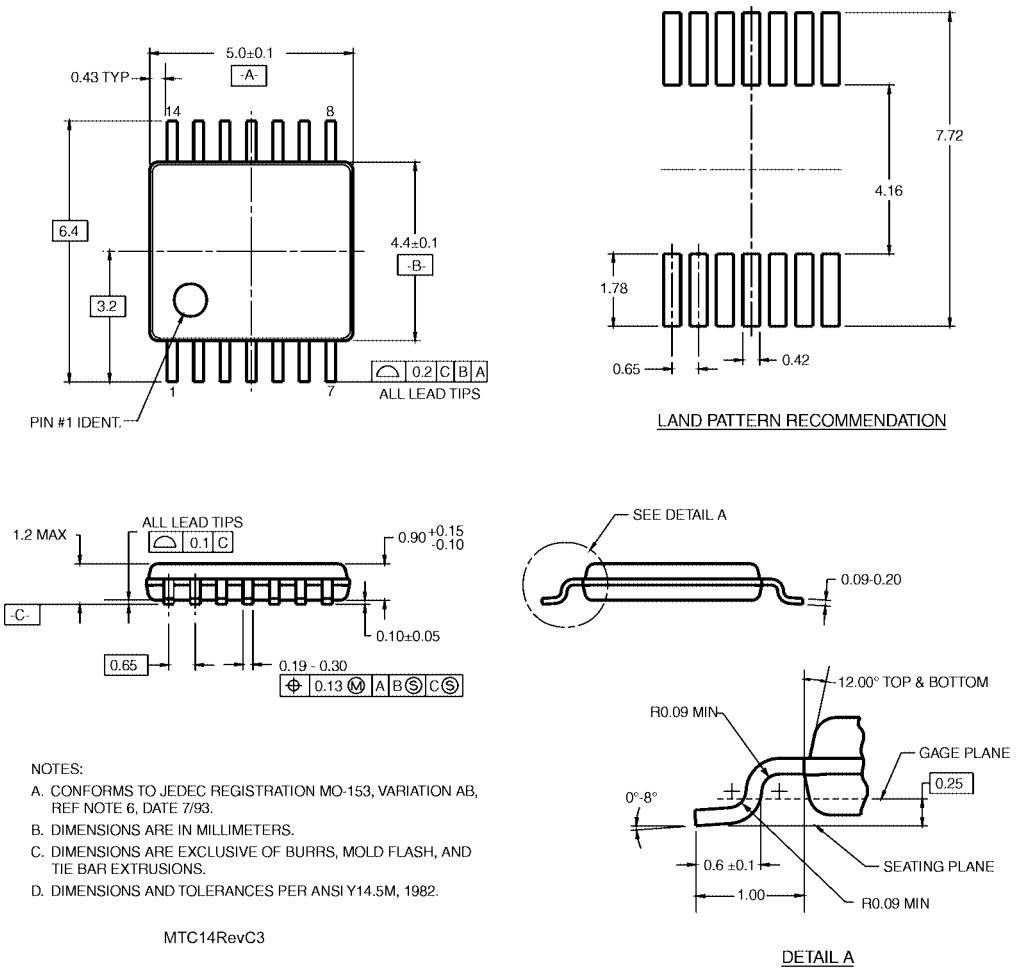
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

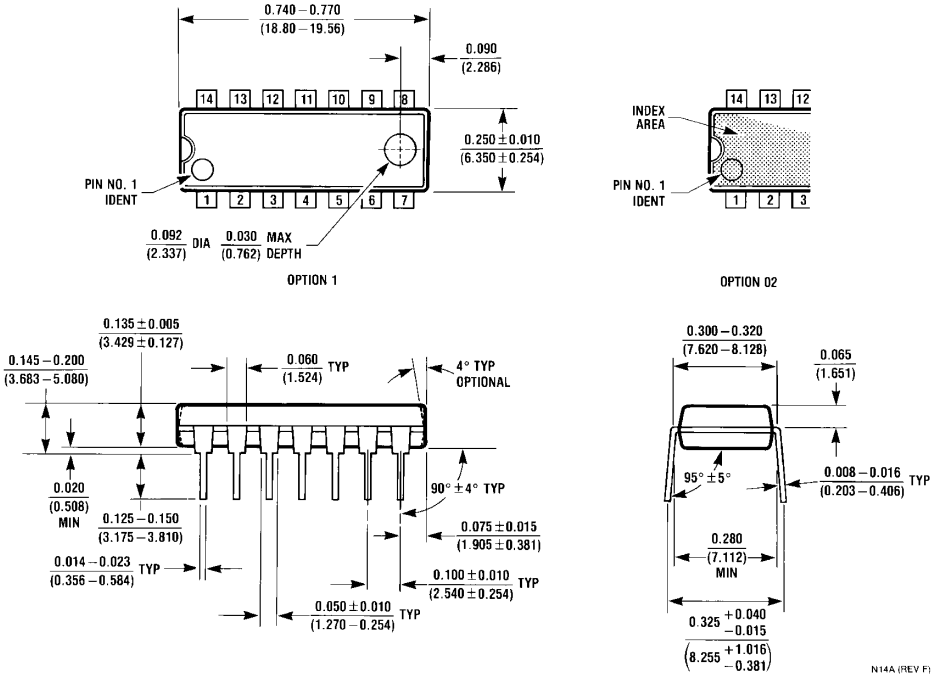
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A